WHAT IS CLAIMED IS:

1. A memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin structure formed on the insulating layer, the fin structure having a first and second side surface;

a first spacer formed adjacent the first side surface, the first spacer acting as a first floating gate for the memory device;

a second spacer formed adjacent the second side surface, the second spacer acting as a second floating gate for the memory device;

a gate dielectric layer formed on the first and second spacers;

a first gate formed on the insulating layer and disposed on a first side of the fin; and

a second gate formed on the insulating layer and disposed on a second side of the fin opposite the first side.

2. The memory device of claim 1, further comprising:

a source region and a drain region formed on the insulating layer and disposed adjacent a respective first and second end of the fin structure.

3. The memory device of claim 2, further comprising:

an oxide layer formed on the first and second side surfaces of the fin, the oxide layer acting as a tunnel oxide layer for the memory device.

4. The memory device of claim 3, wherein the oxide layer has a width ranging from about 10 Å to about 100 Å.

5. The memory device of claim 1, wherein the first and second gates are associated with corresponding memory cells that may be programmed independently of each other.

6. The memory device of claim 1, wherein each of the first and second spacers comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

7. The memory device of claim 1, further comprising:

a dielectric cap comprising at least one of a nitride and an oxide formed over a top surface of the fin structure.

8. The memory device of claim 1, wherein the insulating layer comprises a buried oxide layer and the fin structure comprises at least one of silicon and germanium.

9. The memory device of claim 8, wherein the fin structure has a width ranging from about 100 Å to about 1000 Å.

10. A method of manufacturing a non-volatile memory device, comprising:

forming a fin on an insulating layer, the fin including first and second side surfaces and a top surface;

forming a first dielectric layer on the first and second side surfaces of the fin;

forming source and drain regions;

forming first and second spacers adjacent the respective first and second side surfaces of the fin and abutting the dielectric layer, the first and second spacers acting as floating gates for the non-volatile memory device;

forming a second dielectric layer on the first and second spacers;

depositing a gate material over the insulating layer, the second dielectric layer, the first and second spacers and the fin;

planarizing the gate material; and

patterning and etching the gate material to form a first control gate and a second control gate adjacent the first and second spacers, respectively.

11. The method of claim 10, further comprising:

forming a dielectric cap over the fin.

12. The method of claim 10, wherein the forming the first and second spacers comprises:

depositing a polysilicon layer over the insulating layer and the fin, and

etching the polysilicon layer, wherein the width of the first and second spacers ranges from about 100 Å to about 500 Å.

13. The method of claim 10, wherein the forming a first dielectric layer comprises:

thermally growing an oxide on the first and second side surfaces, wherein the oxide acts as a tunnel oxide for the non-volatile memory device.

14. A non-volatile memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having first and second side surfaces and a top surface;

an oxide layer formed on the first and second side surfaces of the conductive fin;

a first spacer formed adjacent the first side surface of the fin, the first spacer acting as a first floating gate electrode; and

a first gate formed on the insulating layer, the first gate acting as a first control gate for the non-volatile memory device.

15. The non-volatile memory device of claim 14, further comprising:

a second spacer formed adjacent the second side surface of the fin, the second spacer acting as a second floating gate electrode; and

a second gate formed on the insulating layer, the second gate acting as a second control gate for the non-volatile memory device.

16. The non-volatile memory device of claim 15, wherein the first and second gates are formed on opposite sides of the conductive fin and are electrically isolated from each other.

17. The non-volatile memory device of claim 15, wherein the first and second spacers each comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

18. The non-volatile memory device of claim 14, further comprising:

a dielectric cap formed on the top surface of the conductive fin.

19. The non-volatile memory device of claim 14, wherein the oxide layer acts as a tunnel oxide for the memory device and the width of the oxide layer ranges from about 10 Å to about 100 Å.

20. The non-volatile memory device of claim 14, wherein the insulating layer comprises a buried oxide layer and the conductive fin comprises at least one of silicon and germanium.